

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Kiyoshi Kato Art Unit : Unknown
Serial No. : 10/595,567 Examiner : Unknown
Filed : April 27, 2006 Conf. No. : 2837
Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND DESIGN METHOD
 THEREOF

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Supplemental to the Information Disclosure Statement (IDS) filed April 27, 2006, Applicants submit the attached corrected form PTO-1449. The corrected form PTO-1449 is being submitted to correct a typographical error in reference Desig. ID "AS". The attached form PTO-1449 includes the corrected information in bold type.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/28/06


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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-335US1	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Kiyoshi Kato	
		Filing Date April 27, 2006	Group Art Unit

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0083398 A1	06/27/2002	Takeyama et al.			03/30/2001
	AB	2003/0009727 A1	01/09/2003	Takeyama et al.			09/09/2002
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	AE	2005/0250266 A1	11/10/2005	Yamazaki et al.			07/12/2005
	AF	5,705,829	01/06/1998	Miyanaga et al.			01/26/1996
	AG	5,939,731	08/17/1999	Yamazaki et al.			01/08/1997
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Foreign Patent Documents or Published Foreign Patent Applications							
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes No
	AP	11-154169	06/08/1999	JAPAN			AB
	AQ						

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AR	Buyeol Lee et al.; "A CPU on a Glass Substrate Using CG-Silicon TFTs"; <i>ISSCC 2003 / Session 9 / TD: Digital Architecture and Systems / Paper 9.4(Digest of Technical Papers)</i> – IEEE International Solid-State Circuits Conference Vol. 1; pp. 164-165; February 11, 2003
	AS	David Van Campenhout et al., "Timing Verification of Sequential Dynamic Circuits"; <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , Vol. 18, No. 5; pp. 645-658; May 1999
	AT	International Search Report (Application No. PCT/JP2004/016174) dated January 25, 2005

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AU	Written Opinion (Application No. PCT/JP2004/016174) dated January 25, 2005

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